WHAT IS CLAIMED IS:

1. A digital signal processing apparatus comprising:

an A/D converter for converting an analog input signal into a digital signal;

a digital filter for performing half-band processing to a sampling output of a digital signal outputted by said A/D converter and for attenuating a frequency component other than a predetermined normal band from a frequency component included in the sampling output; and

an anti-aliasing circuit for suppressing or removing noise having an aliasing band, which is caused by the half-band processing in said digital filter, by using a sign signal outputted from said digital filter.

2. The apparatus according to claim 1, wherein said anti-aliasing circuit determines whether the output from said digital filter, which is subjected to said half-band processing, is a pass signal having the normal band or a pass signal having the aliasing signal, based on a changing period of the sign signal outputted from said digital filter, and suppresses or removes only the pass signal having the aliasing band.

3. The apparatus according to claim 1, wherein said anti-aliasing circuit comprises:

a period measuring circuit for measuring a changing

period of the sign signal outputted by said digital filter;

a threshold holding circuit for holding a period of an intermediate frequency between the normal band and the aliasing band;

a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold which is set to said threshold holding circuit and for outputting a shift control signal when it is determined that the period measured by said period measuring circuit is not larger than the threshold; and

a shift register for shifting a signal which is inputted from said digital filter and is stored, based on said shift control signal, and for suppressing an amplitude of the aliasing noise.

4. The apparatus according to claim 3, wherein said anti-aliasing circuit further comprises a shift value setting register, to which the number of shift bits is set when the signal, which is inputted from said digital filter and is stored, is subjected to shift processing by said shift register.

5. The apparatus according to claim 3, wherein said anti-aliasing circuit further comprises a delay circuit for delaying the output from said digital filter by a delay time which is taken by the measurement by said period

measuring circuit and the comparison calculation by said comparator.

6. The apparatus according to claim 1, wherein said anti-aliasing circuit comprises:

a period measuring circuit for measuring a changing period of the sign signal which is outputted by said digital filter;

a threshold holding circuit for holding a period of an intermediate frequency between the normal band and the aliasing band;

a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold set to said threshold holding circuit and for outputting a clear signal when it is determined that the period is not larger than the threshold; and

a delay circuit for delaying the output from said digital filter by a delay time which is taken by the measurement of said period measuring circuit and the comparison calculation of said comparator and for erasing a signal during delay processing when said clear signal is inputted.

7. A digital signal processing apparatus comprising:

an A/D converter for converting an analog input signal into a digital signal;

a digital filter for performing half-band processing to a sampling output of a digital signal outputted by said A/D converter and for attenuating a frequency component other than a predetermined normal band from a frequency component included in the sampling output;

an edge-detection circuit for detecting an edge of a sign signal which is outputted by said digital filter and for generating a set pulse;

a period measuring circuit for measuring a changing period of the sign signal which is outputted by said digital filter;

a threshold holding circuit for holding a period of an intermediate frequency between a normal band and an aliasing band;

a comparator for comparing and determining whether or not the period measured by said period measuring circuit is larger than the threshold held by said threshold holding circuit and for outputting a reset pulse when it is determined that the period is not larger than the threshold; and

a detection register for inputting said set pulse so as to be in a set state and outputting a first level and for inputting said reset pulse so as to be in said reset state and outputting a second level.